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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,257	10/16/2003	Juan-Antonio Carballo	AUS920030655US1	9980

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EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,257	CARBALLO, JUAN-ANTONIO	
	Examiner	Art Unit	
	Kevin M. Burd	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. This office action, in response to the appeal brief filed 10/23/2007, is a non-final office action.

2. In view of the appeal brief filed on 10/23/2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

David C. Payne

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4-9, 11-16, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Carballo et al (US 7,133,654).

The applied reference has a common assignee and one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 11 and 18, Carballo discloses a communication link for use in a data processing system shown in figure 1. A receiver interface receives a test signal over a communication channel (column 2, lines 50-52). A clock/data recovery (CDR) circuit extracts the clock signal from the received data signal (column 1, lines 27-35). A "debug unit" is configured to determine a bit error rate (BER). Figure 7 shows the jitter level for a required bit-error rate. Correction is done until this required (target) bit error rate is achieved. Figure 2 shows the "debug unit" 20. Figures 3 and 4 disclose the link quality (jitter) measurement 22A. This circuit determines at least one jitter characteristic of the communication link. The "debug unit" further comprises a "test

advisor" that is configured to output a recommendation regarding a "communication problem" based on the BER and at least one jitter characteristic. The "test advisor" 20 is shown in figure 2. The abstract of Carballo discloses the corrected output may be used to adjust the operational characteristic of the link or otherwise evaluate the link for operating margin.

Regarding claim 2, the transmitter will transmit a pattern of data to the receiver.

Regarding claims 4, 5 and 12, Carballo discloses the "test advisor" is configured to perform at least one additional test when the BER exceeds a predetermined threshold and each of the at least one jitter characteristic is acceptable. The jitter estimates shown in figure 3 are continually made. When the BER is not the required level, either high frequency jitter estimate or low frequency jitter estimate is not an acceptable level and further adjustment is necessary. The abstract further discloses correction factors can be applied to the high frequency jitter measurement.

Regarding claims 6 and 13, sampling latches are controlled when a BER is an unacceptable level and low frequency jitter needs to be compensated (column 4, lines 55-61).

Regarding claims 7 and 14, sampling latches are used to oversample the received signal in the face of high frequency jitter (column 4, lines 44-54).

Regarding claims 8 and 15, frequency offset is determined by providing measurements of jitter and BER (column 3, lines 8-32).

Regarding claims 9 and 16, the CDR circuit comprises an edge detector 26 and phase rotator 27.

Regarding claim 19, sampling latches are used to oversample the received signal in the face of high frequency jitter (column 4, lines 44-54) and the frequency offset is determined by providing measurements of jitter and BER (column 3, lines 8-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-6, 11-13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 2003/0202573) in view of Moore et al (US 2004/0205431).

Regarding claims 1, 11 and 18, Yamaguchi discloses a communication link in a data processing system as described in paragraph 0004. The input is received through an interface and the clock is extracted from the received signal (paragraphs 0005 and 0007). At least one jitter characteristic is determined and a bit error rate is calculated (paragraphs 0005 and 0007). These calculations take place in a device. That device is a "debug unit". These measurements and the improved method and device for determining these measurements described in additional embodiments of the described invention discloses jitter characteristics and the BER is output to a user. The use of these measurements is not expressly stated by Yamaguchi. Moore discloses using a BER and jitter characteristic to output a "recommendation regarding a communication

problem". Moore discloses an apparatus for measuring a jitter tolerance of a device under test (abstract). A number of jitter characteristics are determined and a bit error rate is also determined in bit error rate tester 104. Paragraphs 0037 and 0038 disclose changes are made in the device according to the BER and jitter characteristics. A component of the device will output the signal to adjust the device. This component is a "test advisor". By combining the apparatus of Moore into the communication link of Yamaguchi, the receiver can be properly calibrated allowing data to be received with fewer errors.

Regarding claim 2, Moore discloses a pattern generator 100 is used in the communication system.

Regarding claims 4-6, 12 and 13, Moore discloses a test pattern is analyzed by a BERT tester and an additional test is performed when the BER is above a threshold and a jitter characteristic is acceptable (figure 4 and paragraphs 0037-0038).

5. Claims 3, 7-9, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 2003/0202573) in view of Moore et al (US 2004/0205431) further in view of Cranford, JR et al (US 2002/0146084).

Regarding claim 3, the combination of Yamaguchi and Moore discloses the receiver interface converts the serial data to parallel data in paragraphs 0005 and 0007 of Yamaguchi. The combination does not disclose the serial data is non-return to zero (NRZ) formatted serial data. Cranford discloses an apparatus for oversampling data to suppress jitter. Serial data is transmitted across wired media and the data is converted

to parallel data (paragraph 0004). The data is NRZ encoded (paragraph 0015) and the data will be processed by CMOS components (paragraph 0030). The NRZ data has an embedded clock and this clock will add little jitter to the system. NRZ is also a well known method of efficiently and effectively encoding data. For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the teachings of Cranford into the combination of Yamaguchi and Moore.

Regarding claims 7, 14 and 19, the combination of Yamaguchi and Moore discloses the apparatus stated above in paragraph 4. The combination does not disclose the jitter characteristic includes a high frequency jitter and a modification of the sampling is conducted according to the high frequency jitter. Cranford discloses the receiver performs clock and data recovery (CDR) on the incoming serial data stream. Feed forward and feedback controls are combined in the receiver architecture. The data is oversampled. The feed forward section suppresses high frequency jitter. The oversampled data is adjusted according to the sampling phases of the early and late signals (paragraph 0025). The suppression of this jitter is advantageous since the received data will be recovered with fewer errors when the jitter is removed. For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Cranford into the combination of Yamaguchi and Moore.

Regarding claims 8 and 15, the combination of Yamaguchi and Moore discloses the apparatus stated above in paragraph 4. The combination does not disclose the jitter characteristic includes a frequency offset. Cranford discloses the TX and RX frequency

offset is allowed as long as the jitter of the two clocks is small enough. If the frequency offset is not acceptable, the jitter is too high and will be adjusted. This will increase the throughput of the system since data will be lost due to high jitter. By changing the bandwidth of the system, more data will be properly received at the receiver and other downstream elements. For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Cranford into the combination of Yamaguchi and Moore.

Regarding claims 9 and 16, the combination of Yamaguchi and Moore discloses the apparatus stated above in paragraph 4. The combination does not disclose the clock and data recover (CDR) includes an edge detector and phase rotator. Cranford discloses the receiver performs clock and data recovery (CDR) on the incoming serial data stream. The CDR comprises an edge detector and phase rotator (figure 2). Feed forward and feedback controls are combined in the receiver architecture. The data is oversampled. The feed forward section suppresses high frequency jitter. The oversampled data is adjusted according to the sampling phases of the early and late signals (paragraph 0025). The suppression of this jitter is advantageous since the received data will be recovered with fewer errors when the jitter is removed. For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Cranford into the combination of Yamaguchi and Moore.

6. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 2003/0202573) in view of Moore et al (US 2004/0205431) further in view of Francos et al (US 2003/0072388).

Regarding claims 10 and 17, the combination of Yamaguchi and Moore does not disclose a look-up table (LUT). Francos discloses a LUT in a circuit receiving an input signal. The LUT stores data and is accessed according to specified input signals (paragraph 0011). The LUT can store any data. It is useful to store data so calculations can be made prior to implementation of a circuit. Real-time data can be processed quicker since the calculations are completed. For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to include the LUT of Francos into the circuit of the combination of Yamaguchi and Moore.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 2003/0202573) in view of Moore et al (US 2004/0205431) further in view of Cranford, JR et al (US 2002/0146084).

Regarding claim 20, the combination of Yamaguchi, Moore and Cranford does not disclose a look-up table (LUT). Francos discloses a circuit comprising a LUT in an apparatus that receives an input signal. The LUT stores data and that data is accessed according to specified input signals (paragraph 0011). The LUT can store any data and can be accessed by any data that will provide the proper address information to the LUT. It is useful to store data so calculations can be made prior to implementation of a circuit. Real-time data can be processed quicker since the calculations are completed.

For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to include the LUT of Francos into the circuit of the combination of Yamaguchi and Moore.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEVIN BURD
PRIMARY EXAMINER
Kevin M. Burd
1/6/2008